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A −97.2 dB PSR 3.18 ppm/°C Bandgap Voltage Reference with Curvature Compensation

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Abstract

Voltage reference has always been an essential building block in integrated circuits and microsystems, such as communication systems and RF modules, as well as wearable and portable devices. This paper proposes a high-power-supply-rejection (PSR) bandgap reference with curvature compensation in the 180 nm BCD process. A common-mode feedback (CMFB) module is integrated into the classical Brokaw bandgap reference to suppress voltage fluctuations at the amplifier input caused by power supply variations. A high-order curvature compensation circuit is used to achieve a low temperature coefficient (TC) by compensating for the nonlinearity of the base-emitter voltage (V_{BE}). Simulation results indicate that the circuit realizes a maximum TC of 3.2 ppm/°C from −40 °C to 125 °C with an output voltage of 1.2 V, and an average PSR of −97.2 dB at 100 Hz.

Keywords: bandgap reference; high PSR; curvature compensation

1. Introduction

Bandgap reference (BGR) circuits are key components in most integrated microsystems that contain analog or mixed-signal circuits, providing stable and precise voltage references [1–4]. For example, the signal-processing accuracy of high-performance analog systems such as sensor circuits heavily relies on stable and accurate voltage references. In recent years, the rapid growth of wearable devices, portable devices, as well as medical implants has increased the requirements for signal processing accuracy of microsystems; achieving a bandgap reference with both high PSR and low TC has become a challenge [5–8].

Conventional BGR designs encounter challenges in achieving a low TC. First-order temperature compensation, commonly used in traditional designs like the Brokaw bandgap reference, is insufficient to meet the stringent demands of modern applications due to the nonlinear temperature dependence of the base-emitter voltage (V_{BE}). To address this limitation, an increasing number of designs incorporate high-order curvature compensation to effectively reduce TC [9–12].

While numerous studies have proposed high-PSR bandgap reference circuits using techniques such as cascode structures and pre-regulators [13–20], theoretical analyses of PSR-enhancement methods are comparatively few. Moreover, existing approaches often lead to increased circuit complexity and large area consumption.

This paper proposes a novel bandgap reference design that achieves both high PSR and low TC by integrating a CMFB module and employing high-order curvature compensation. The CMFB module stabilizes the input voltages of the amplifier against power-supply fluctuations. The CMFB module only requires a single-stage differential amplification chain.

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By mapping common-mode variations of critical nodes directly to the top current generator, the PSR is improved without compromising the voltage headroom. Simultaneously, a high-order curvature compensation is introduced to mitigate the nonlinearity of V_{BE}, resulting in a low TC.

The paper is organized as follows: Section 2 introduces the proposed circuit and provides theoretical analyses of PSR and TC optimization. Section 3 presents the simulation results. The conclusions are included in Section 4.

2. Circuit Implementation

The structure of the proposed bandgap reference is shown in Figure 1, which contains a CMFB module, a curvature compensation module, and a bandgap core circuit. The specific circuit of the proposed structure is shown in Figure 2 in detail.

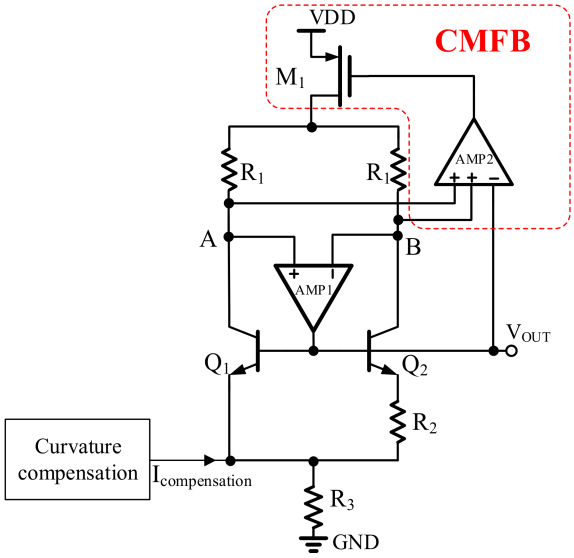


Figure 1. Proposed bandgap reference structure.

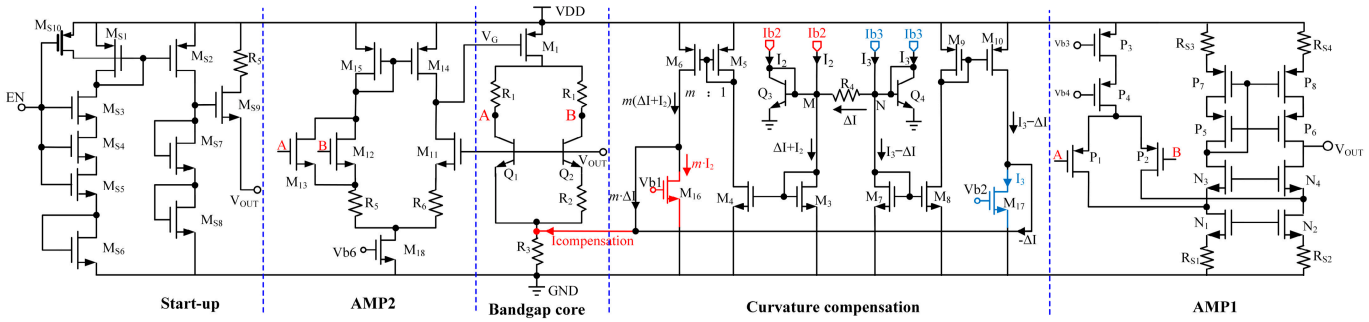


Figure 2. Detailed circuit schematic of the proposed bandgap.

2.1. High Power Supply Rejection Analysis and Design

As shown in Figure 3, the output voltage of the classical Brokaw bandgap is affected by the PSR of AMP1 and voltage variations at nodes A and B. Variations of V_A and V_B are affected by the supply voltage and the output reference voltage (V_{OUT}).

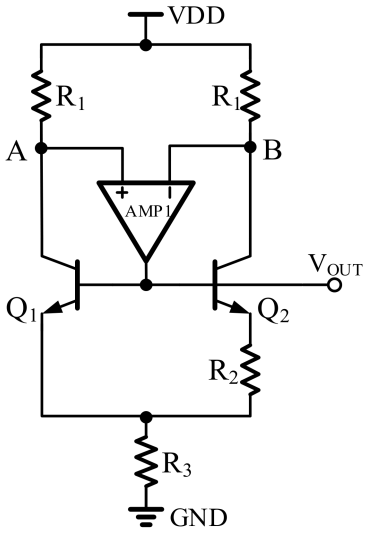


Figure 3. Classical Brokaw bandgap structure.

VDD affects V_A and V_B through the voltage divider shown in Figure 4a, where β_{1A} is the gain of VDD to V_A, β_{1B} is the gain of VDD to V_B; R_A denotes the effective impedance from V_A to GND, and R_B denotes the effective impedance from V_B to GND.

$$\beta_{1A} = \frac{R_A}{R_1 + R_A} \tag{1}$$

$$\beta_{1B} = \frac{R_B}{R_1 + R_B} \tag{2}$$

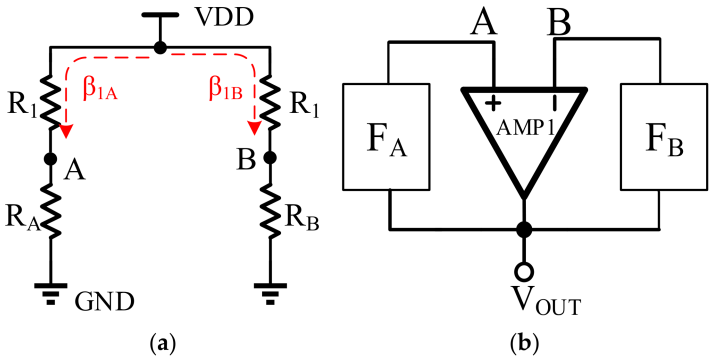


Figure 4. (**a**) Voltage divider; (**b**) Feedback network of the Brokaw BGR.

V_{OUT} affects V_A and V_B through a feedback network shown in Figure 4b, where F_A is a common-emitter (CE) circuit composed of Q_1, R_1, and R_3 with a gain of β_{2A}; F_B is a CE circuit composed of Q_2, R_1, R_2, and R_3 with a gain of β_{2B}.

$$\beta_{2A} = -\frac{R_1}{2R_3} \tag{3}$$

$$\beta_{2B} = -\frac{R_1}{R_2 + 2R_3} \tag{4}$$

$$\Delta V_{OUT} = A_d(\Delta V_{d,VDD} + \Delta V_{d,OUT}) + A_{cm}(\Delta V_{cm,VDD} + \Delta V_{cm,OUT}) + PSR_{AMP1} \cdot \Delta V_{DD} \tag{5}$$

The final output voltage variation is shown in Equation (5), where ΔV_{VDD} represents variations in the power supply, ΔV_{OUT} represents the variation of the output, A_d represents the differential-mode gain, A_{cm} represents the common-mode gain, and PSR_{AMP1}

represents the PSR of AMP1. $\Delta V_{d,VDD}$ denotes the difference between V_A and V_B due to VDD variation, $\Delta V_{d,OUT}$ denotes the difference between V_A and V_B due to V_{OUT} variation, $\Delta V_{cm,VDD}$ denotes the common-mode variation between V_A and V_B due to VDD variation, and $\Delta V_{cm,OUT}$ denotes the common-mode variation between V_A and V_B due to V_{OUT} variation, which can be expressed by

$$\Delta V_{d,VDD} = (\beta_{1A} - \beta_{1B}) \times \Delta V_{DD} \tag{6}$$

$$\Delta V_{d,OUT} = (\beta_{2A} - \beta_{2B}) \times \Delta V_{OUT} \tag{7}$$

$$\Delta V_{cm,VDD} = \Delta V_{DD} \times (\beta_{1A} + \beta_{1B})/2 \tag{8}$$

$$\Delta V_{cm,OUT} = \Delta V_{OUT} \times (\beta_{2A} + \beta_{2B})/2 \tag{9}$$

For simplicity, use $\Delta\beta_n$ to represent $(\beta_{nA} - \beta_{nB})$; use $\overline{\beta}_n$ to represent $(\beta_{nA} + \beta_{nB})/2$. Take Equations (6)~(9) into Equation (5); the ratio of ΔV_{OUT} to ΔV_{DD} can be expressed as

$$\begin{aligned} \frac{\Delta V_{OUT}}{\Delta V_{DD}} &= A_d \times (\Delta\beta_1 + \Delta\beta_2 \cdot \frac{\Delta V_{OUT}}{\Delta V_{DD}}) + A_{cm}(\overline{\beta}_1 + \overline{\beta}_2 \cdot \frac{\Delta V_{OUT}}{\Delta V_{DD}}) + PSR_{AMP1} \\ &= \frac{A_d \times \Delta\beta_1 + A_{cm} \times \overline{\beta}_1 + PSR_{AMP1}}{1 - A_d \times \Delta\beta_2 - A_{cm} \times \overline{\beta}_2} \end{aligned} \tag{10}$$

PSR of the classical Brokaw bandgap reference can be shown as

$$\begin{aligned} PSR &= 20\lg(\frac{\Delta V_{OUT}}{\Delta V_{DD}}) = 20\lg(\frac{A_d \times \Delta\beta_1 + A_{cm} \times \overline{\beta}_1 + PSR_{AMP1}}{1 - A_d \times \Delta\beta_2 - A_{cm} \times \overline{\beta}_2}) \\ &= 20\lg(\frac{\Delta\beta_1 + \frac{\overline{\beta}_1}{CMRR_{AMP1}} + \frac{PSR_{AMP1}}{A_d}}{\frac{1}{A_d} - \Delta\beta_2 - \frac{\overline{\beta}_2}{CMRR_{AMP1}}}) \end{aligned} \tag{11}$$

where $CMRR_{AMP1}$ is the common-mode rejection ratio, defined as the ratio of differential-mode gain A_d to common-mode gain A_{cm}.

To achieve a better PSR, the parameters $\frac{\overline{\beta}_1}{CMRR_{AMP1}}$ and $\frac{PSR_{AMP1}}{A_d}$ in Equation (11) should ideally approach 0. This necessitates a reference circuit with an infinite CMRR, infinite differential-mode gain (A1), and robust PSR of AMP1.

To enhance the PSR of the reference circuit in terms of CMRR, two strategies can be employed. Firstly, the internal circuit structure of AMP1 can be optimized to minimize common-mode gain or maximize differential-mode gain. A common method to improve A1 and PSR is the use of cascode configurations. Secondly, supplementary modules can be introduced to stabilize the input voltage, thereby indirectly enhancing common-mode rejection. Therefore, a CMFB module can be incorporated, as shown in Figure 5, where AMP2 and M_1 form the CMFB module.

The operation of this CMFB can be analyzed as follows. Firstly, an increase in VDD elevates the common-mode voltages of nodes A and B. These voltages serve as in-phase inputs of AMP2, resulting in an amplified output that increases the gate voltage of M_1. With the introduction of AMP2, the elevated gate voltage of M_1 reduces the current through M_1, consequently lowering the common-mode voltages at nodes A and B. Secondly, an increase in V_{OUT} reduces the voltages at nodes A and B via the two common-emitter circuits, F_A and F_B, as depicted in Figure 4b. This decrease in the positive input voltages of AMP2, coupled with an increase in the negative input voltage, leads to a reduction in the gate voltage of M_1 following differential amplification by AMP2. As a result, the currents through the branches containing Q_1 and Q_2 increase, causing the voltages at nodes A and B to rise.

The CMFB module in this work only requires a single-stage differential amplification chain, which does not damage the main pole architecture of the main loop. By mapping the common-mode variations of core nodes directly to the top current generator, strict supply-voltage overhead is avoided.

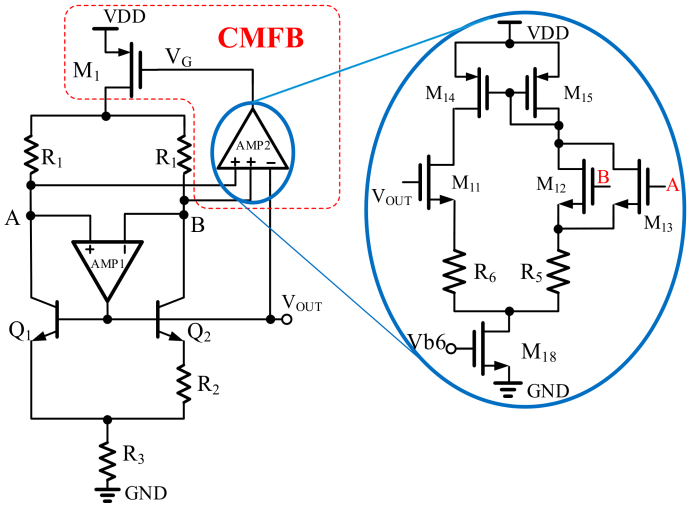


Figure 5. CMFB consists of AMP2 and M1.

The proposed structure includes a Brokaw feedback loop which contains AMP1, and a CMFB regulation loop which contains AMP2. The loops must be designed properly to avoid stability issues. The main purpose of the CMFB module is to eliminate power fluctuations at low frequency; therefore, AMP2 is a low-bandwidth, high-DC-gain architecture to make the CMFB loop act as a slow loop. The main Brokaw loop acts as a fast loop; therefore, the bandwidth of AMP1 must be sufficiently larger than that of AMP2. Miller compensation capacitor is utilized to limit the frequency of the main pole of AMP2. As a result, complete decoupling of the main loop and common-mode loop can be achieved in the frequency domain.

2.2. Curvature Compensation

High-order curvature compensation is employed to compensate for the nonlinearity of V_{BE}, as described in Equation (12) [21]. To eliminate this nonlinearity, a positive term $V_T \ln \frac{T}{T_0}$ should be introduced through curvature compensation [22].

The expression for $V_{BE}(T)$ of a BJT is presented in Equation (12), where V_{g0} is the silicon bandgap voltage at 0 K [23], η is a process-dependent parameter independent of temperature [24], and α is a parameter determined by the temperature coefficient of the bias current flowing through the BJT. Specifically, α equals 1 when the bias current exhibits a positive TC and 0 when the bias current has a zero TC [25].

$$V_{BE}(T) = V_{g0} - (V_{g0} - V_{BE0})\frac{T}{T_0} - (\eta - \alpha)V_T \ln \frac{T}{T_0} \quad (12)$$

$$V_{OUT} = 2\frac{R_3}{R_2}V_T \ln N + V_{BE1} \quad (13)$$

The proposed curvature compensation circuit is illustrated in Figure 6. The current I_2 flowing through Q_3 is a constant current, whereas the bias current I_3 flowing through Q_4 is proportional to the absolute temperature (PTAT) current. The V_{BE} expressions of Q_3 and Q_4 are provided in Equations (14) and (15), respectively. By taking the difference between the V_{BE} of Q_3 and Q_4, the required term is obtained, as shown in Equation (16). This voltage is converted into a current ΔI via resistor R_4 as expressed in Equation (17).

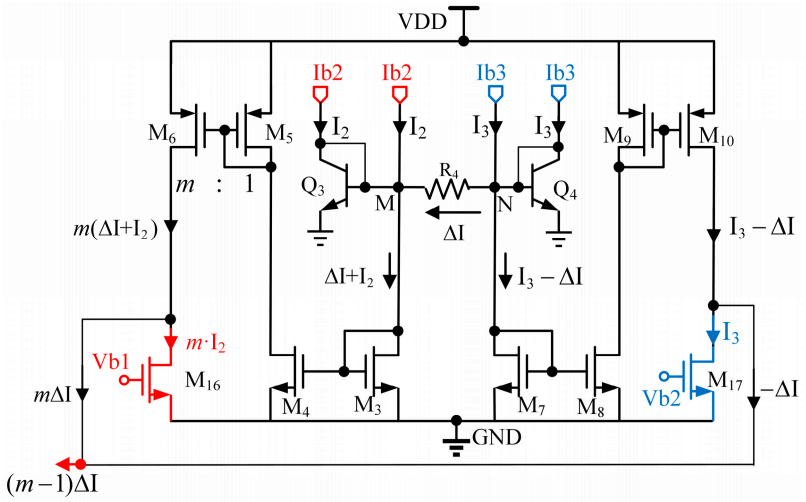


Figure 6. Curvature compensation circuit.

As depicted in Figure 6, the current flowing through M_3 is $\Delta I + I_2$. This current is mirrored and scaled to $m(\Delta I + I_2)$ by the current mirror comprising M3–M6, where M_5 and M_6 are designed with a ratio of 1: m. Similarly, the current mirror M_7–M_{10} replicates the current $I_3 - \Delta I$ flowing through M_7. The total compensation current is composed of the sum of two components, $m\Delta I$ and $-\Delta I$, as expressed in Equation (18).

$$V_{BE,Q_4}(T) = V_{g0} - (V_{g0} - V_{BE0})\frac{T}{T_0} - (\eta - 1)V_T \ln\frac{T}{T_0} \tag{14}$$

$$V_{BE,Q_3}(T) = V_{g0} - (V_{g0} - V_{BE0})\frac{T}{T_0} - \eta V_T \ln\frac{T}{T_0} \tag{15}$$

$$\Delta V_{BE,Q_4-Q_3}(T) = V_T \ln\frac{T}{T_0} \tag{16}$$

$$\Delta I = \frac{V_T \ln T/T_0}{R_4} \tag{17}$$

$$I_{compensation} = (m-1)\Delta I = \frac{m-1}{R_4} V_T \ln T/T_0 \tag{18}$$

With the incorporation of the curvature compensation module, the output voltage of the bandgap reference is adjusted from Equation (13) to Equation (19).

$$V_{OUT} = 2\frac{R_3}{R_2} V_T \ln N + V_{BE1} + \frac{R_3}{R_4}(m-1)V_T \ln\frac{T}{T_0} \tag{19}$$

By substituting the temperature-dependent expression of V_{BE} given in Equation (12) into Equation (19), we obtain Equation (20).

$$V_{OUT} = 2\frac{R_3}{R_2}\frac{kT}{q}\ln N + [V_{g0} - (V_{g0} - V_{BE0})\frac{T}{T_0} - (\eta - \alpha)\frac{kT}{q}\ln\frac{T}{T_0}] + \frac{R_3}{R_4}(m-1)\frac{kT}{q}\ln\frac{T}{T_0} \tag{20}$$

Taking the derivative of Equation (20) with respect to temperature yields Equation (21).

$$\frac{dV_{OUT}}{dT} = 2\frac{R_3}{R_2}\frac{k}{q}\ln N - \frac{V_{g0} - V_{BE0}}{T_0} + [\frac{R_3}{R_4}(m-1) - (\eta - \alpha)]\frac{k}{q}(\ln\frac{T}{T_0} + 1) \tag{21}$$

Since only the last term of Equation (21) contains the temperature variable, setting Equation (21) to zero yields only one solution. Therefore, this compensation approach leads to a temperature curve with a single zero-slope point under ideal conditions. The

temperature value corresponding to zero slope in the output curves before and after curvature compensation is different, which results from the different coefficients of the temperature variable in the last term of Equation (21).

With properly designed values of m and the ratio of resistors, the influence of high-order nonlinear temperature terms on the reference voltage can be effectively weakened. To minimize layout-induced mismatch non-idealities, m and the ratio of resistors should be restricted to integers. The objective is to perfectly neutralize the non-linear component of V_{BE} at the central temperature node, achieving the minimum temperature coefficient. Therefore, the zero-slope point should be located around the middle of the concerned temperature span.

2.3. Bias Circuit

Figure 7 illustrates the bias-generation circuit employed in the curvature compensation module. In the PTAT current generator, the bandgap reference output voltage is connected to the base of transistor Q_{C5}. Since the base–emitter voltage V_{BE} of Q_{C5} has a negative temperature coefficient and V_{OUT} is temperature independent, the emitter voltage of Q_{C5}, which corresponds to the voltage across resistor R_{C2}, shows a positive temperature coefficient. The current flowing through R_{C2} therefore has a positive temperature coefficient. This current is mirrored by transistors Q_{C1}~Q_{C3} to generate a PTAT current I_3. The bias voltage Vb2 is applied to the gate of M_{17} in Figure 6. AMP3 and AMP4 are employed as clamping amplifiers. In AMP4, the gate voltage V_G of M_{C1} is driven by the output of the CMFB amplifier AMP2, which also controls the gate of M_1. Under normal operation of the CMFB module, M_1 in Figure 5 and M_{C1} in Figure 7 are simultaneously biased on.

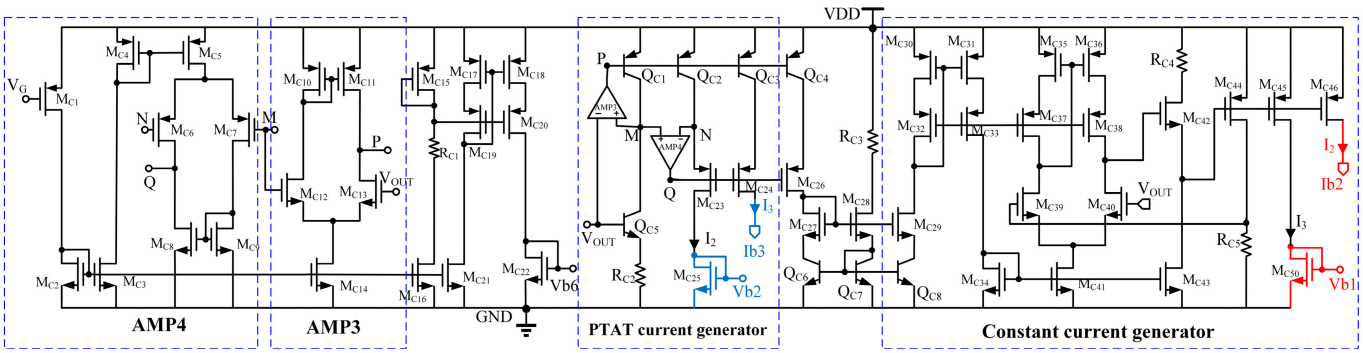


Figure 7. Bias generator for curvature compensation.

In the constant-current generator, the amplifier formed by M_{C35}~M_{C44}, R_{C4}, and R_{C5} provides strong negative feedback, forcing the inverting input at the gate of M_{C39} to closely track the non-inverting input voltage V_{OUT}. Therefore, under temperature variations, the voltage across R_{C5} remains approximately constant. The resulting nearly constant current is then mirrored by the current mirror formed by M_{C45}~M_{C46} to generate I_2. This current is used to generate the bias voltage Vb1, which is applied to the gate of M_{16} in Figure 6, and M_{16} mirrors the PTAT current with a scaling factor of m.

3. Post-Layout Simulation Results

The proposed BGR circuit is implemented using the 0.18 um process and occupies an active area of 0.118 mm^2, which is depicted in Figure 8.

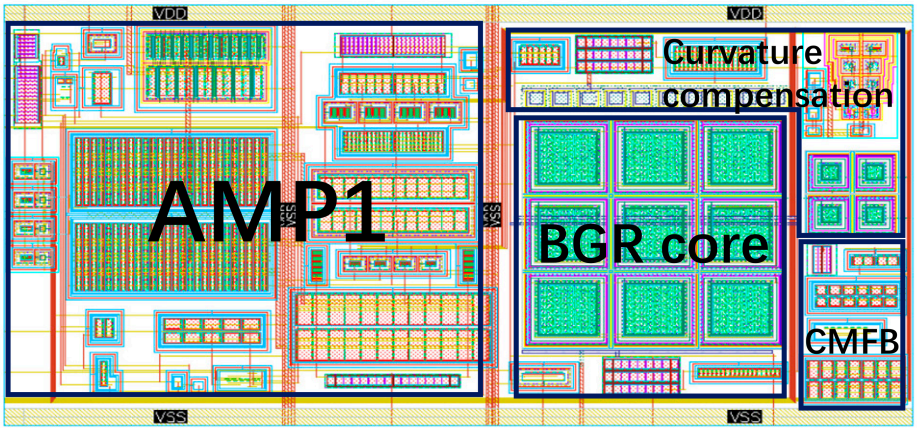


Figure 8. The layout of the proposed BGR.

The proposed design shows load regulation of 2.14~2.6 mV/mA across process corners, and 2.28 mV/mA at the tt corner. Figure 9 shows the post-simulation result of output voltage from −40 to 125 °C at process corners. The tt, ff, ss, sf, and fs corners present TC of 3.07 ppm/°C, 2.63 ppm/°C, 1.66 ppm/°C, 2.62 ppm/°C, and 3.18 ppm/°C, respectively. The appearance of multiple zero-slope points under the ff and ss process corners is not an intended design feature. Instead, they result from process variations. Actually, the single zero-slope expression is derived with an ideal device model, which assumes the temperature has no effect on the gain of amplifiers, BJT ratios, and resistance ratios, which will all appear in the layout simulation. Moreover, I_2 and I_3 are not ideal constant current or PATA current, and they are actually generated on the basis of V_{OUT}, which is temperature-dependent itself. In other words, the effect of temperature on parameter α can emerge under extreme processes. However, the TC is not degraded under extreme processes; therefore, practical application is not affected.

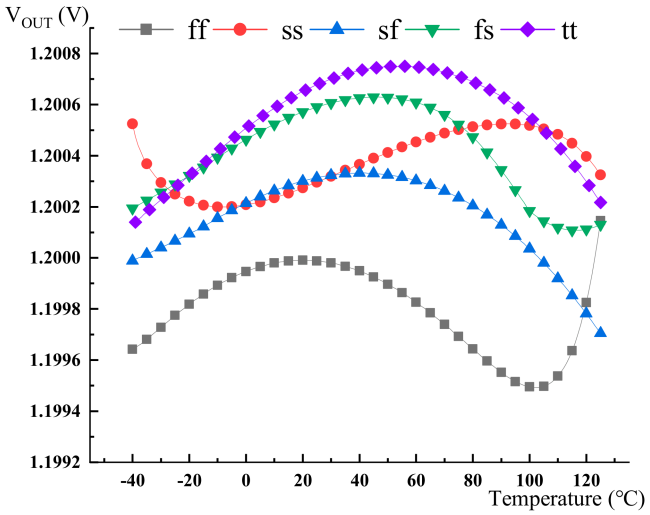


Figure 9. The V_{OUT}-T curve at different process corners.

Figure 10 compares the output V_{OUT}-T curves from −40 °C to 125 °C with and without curvature compensation at process corners. At tt corner, the TC is 3.07 ppm/°C with curvature compensation and 7.57 ppm/°C without curvature compensation, and the zero-slope temperature changes when curvature compensation is applied. This originates from the additional coefficient in the last temperature-dependent term of Equation (21); the value of T making dV_{OUT}/dT equal to 0 is actually increased when the compensation

term is introduced. Furthermore, because the original nonlinear temperature component in Equation (20) is compensated, the voltage shows a smaller variation over temperature.

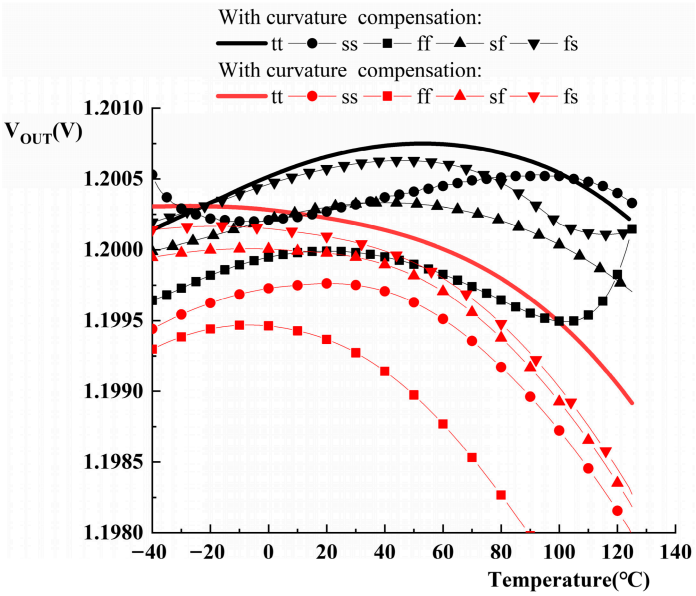


Figure 10. Comparison between V_{OUT} with and without curvature compensation.

Figure 11 is the output voltage distribution obtained from 500-point Monte Carlo analyses, with an average output voltage of 1.20026 V and a standard deviation of 0.209 mV.

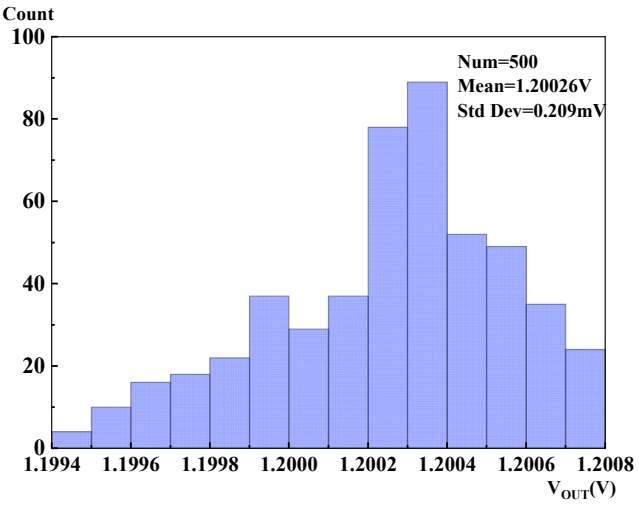


Figure 11. 500-point Monte Carlo simulation results of V_{OUT}.

Figure 12 presents a comparison between the PSR performance with and without CMFB. At the TT corner, the low-frequency PSR is −59 dB without CMFB and improves significantly to −96.2 dB with CMFB, which validates the theoretical analysis of PSR and demonstrates that the incorporation of CMFB enhances the PSR performance of the classical Brokaw bandgap. Actually, the PSR roll-off arises when the CMFB loop gain drops with frequency. As discussed earlier, the bandwidth of AMP2 is designed to be very low. As frequency increases, the CMFB loop gain drops and disturbance is no longer suppressed.

Miller compensation in AMP2 results in a low frequency of the dominant pole; therefore, the gain of AMP2 A_{AMP2} can be approximated by

$$A_{AMP2}(s) = \frac{A_{dc,2}}{1 + \frac{s}{\omega_{p2}}} \tag{22}$$

where $A_{dc,2}$ is the DC gain of AMP2 and ω_{p2} is the dominant pole of AMP2. The load impedance at M1 drain can be expressed as

$$Z_{AB}(s) = R_{eq} || \frac{1}{sC_{para}} = \frac{R_{eq}}{1 + sR_{eq}C_{para}} \tag{23}$$

where R_{eq} and C_{para} are the equivalent resistance and parasitic capacitance seen at M1 drain. Assuming g_{m1} is the transconductance of M1, the CMFB loop gain $G_{CMFB}(s)$ can be expressed as

$$G_{CMFB}(s) = A_{AMP2}(s) \cdot g_{m1} \cdot Z_{AB}(s) = \frac{A_{dc,2} g_{m1} R_{eq}}{\left(1 + \frac{s}{1 / R_{eq}C_{para}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{24}$$

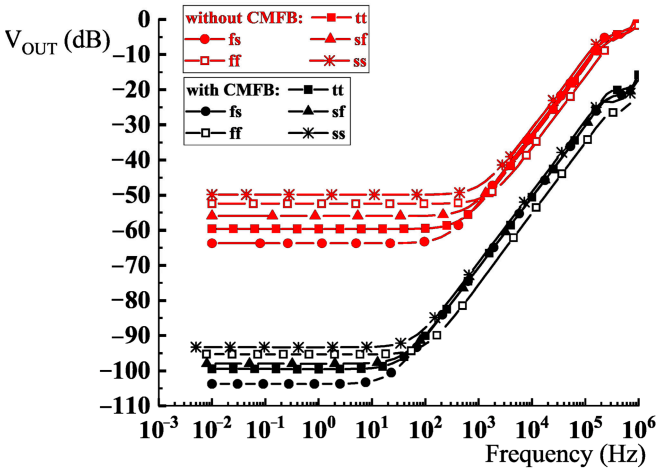


Figure 12. The PSR performance with and without CMFB across corners.

There are two poles in the approximated loop gain. However, the dominant pole of AMP2 is limited to be very low through Miller compensation to form a slow loop; therefore, ω_{p2} is much smaller than $\frac{1}{R_{eq}C_{par}}$ and the PSR corner frequency is limited by the bandwidth of AMP2.

Figure 13 is the PSR distribution at 100 Hz obtained from 500-point Monte Carlo analyses of the proposed BGR circuit, with an average PSR of −97.2 dB and a standard deviation of 1.72 dB.

The loops must be designed properly to avoid stability risks. The Bode plot for both the main loop and CMFB loop across process corners and temperature extremes is shown in Figure 14. Since Miller compensation is adopted to limit the frequency of the main pole of AMP2, the bandwidth of the CMFB loop is an order of magnitude smaller than that of the main loop, achieving decoupling of the main loop and common-mode loop in the frequency domain.

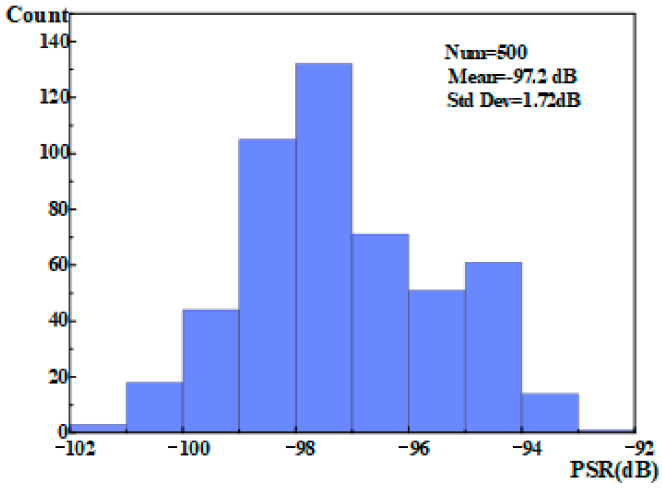


Figure 13. 500-point Monte Carlo simulation results of PSR at 100 Hz.

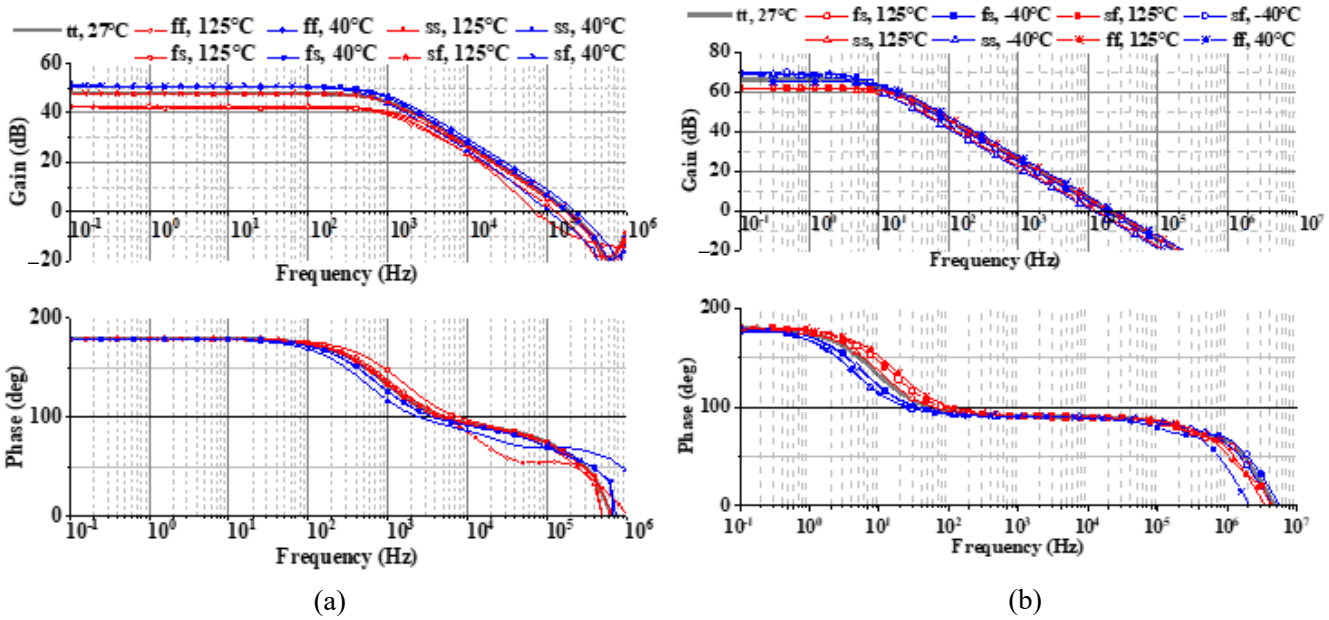


Figure 14. Bode plot for the loop gain: (**a**) Brokaw loop; (**b**) CMFB loop.

It is necessary to mention that the results are based on post-layout simulations. Non-idealities could degrade the real-chip performance. For example, at elevated temperatures, leakage current from the current mirrors can become significant, which injects directly into node A/B or the bipolar transistors. The TC curve relies on the ratio through Q_1/Q_2 and the compensation current, both of which will be corrupted by the leakage current. Furthermore, the decrease in differential-mode gain and CMRR will degrade PSR. On the other hand, unpredictable packaging stress could induce physical mismatch in internal resistors and transistors, resulting in absolute drift in the output voltage and severe degradation of the temperature coefficient. Figure 15 depicts the effect of a 2 mV offset voltage V_{os} at the input pairs of AMP1 and the BJT pairs (Q1, Q2 and Q3, Q4). Mathematically, V_{os} at the AMP1 input will only add a small DC term to the output voltage through ΔV_{be}; therefore, TC is not influenced. V_{os} at Q_1/Q_2 pairs causes significant degradation of V_{OUT}, because it is magnified to about 20 mV by the amplification factor of the PTAT term V_{OUT} in Equation (13). V_{os} at Q_3/Q_4 pairs degrades the TC to 8 ppm/°C because the term for compensation in Equation (20) is disturbed. However, in real chips, V_{os} is actually strongly temperature-dependent, and the TC could be a very complex nonlinear

function. In addition, real-world chips suffer from unavoidable overlapping random offsets; therefore, trimming is necessary.

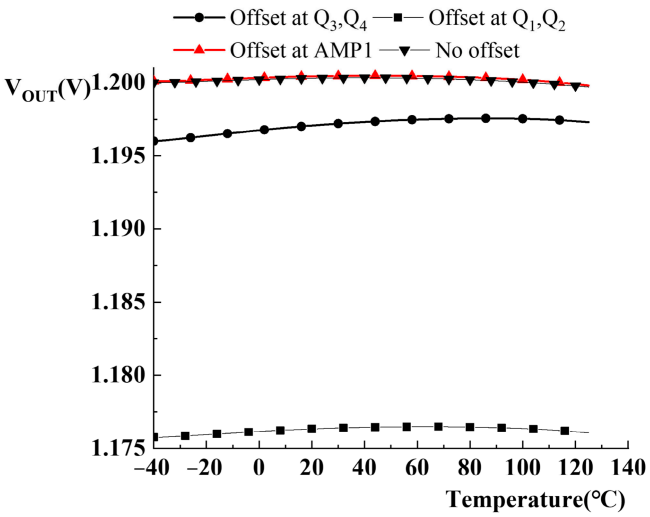


Figure 15. Simulated V_{OUT} with offset voltages of 2 mV.

Table 1 summarizes the performance of the proposed BGR in comparison to other reported results. The proposed design achieves both a combination and a balance of high PSR and low TC while maintaining a compact layout area.

Table 1. Performance comparison.

	[9]	[16]	[26]	[27]	[28]	[29]	This Work
Process (μm)	0.18	0.18	0.18	0.11	0.18	0.18	0.18
Vref (V)	1.038	1.245	1.21	1.2	1.65	1.25	1.2
Tem. Range (°C)	−55~125	−40~130	−32~135	−40~125	−40~125	−45~125	−40~125
TC (ppm/°C)	0.2	3.25	0.7~1.16	2.18	2.2~6.2	4.2	1.66~3.18
PSR (dB) @100 Hz	−71	−103	−89	N/A	−68	−100	−97.2
Quiescent current (μA)	49	N/A	N/A	N/A	N/A	N/A	32
Power (μW)	161.7	13.2	N/A	N/A	N/A	127.8	160
Line Regulation (%/V)	N/A	N/A	N/A	N/A	0.18	0.012	0.27
Active area (mm^2)	0.01	0.56	0.0695	N/A	0.329	1.3	0.118

4. Conclusions

A low TC, high-PSR bandgap reference with curvature compensation is proposed and implemented by the 180 nm BCD process in this paper. The design incorporates high-order curvature compensation to reduce nonlinearity in VBE, and employs a common-mode feedback module to enhance the PSR performance. As a result, the proposed reference achieves a maximum TC of 3.18 ppm/°C over a temperature range from −40 °C to 125 °C across process corners. Furthermore, compared to the conventional Brokaw topology, the PSR at 100 Hz is significantly improved from −59 dB to −96.2 dB with the introduction of the common-mode feedback module. These results demonstrate that the proposed architecture achieves a well-balanced combination of wide temperature stability, high PSR, and compact layout, making it a practical solution for high-precision sensor interface systems such as medical implants, aerospace, and Internet of Things (IoT).

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